REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed September 14, 2004. In the Office Action, the Examiner rejected claims 1- 30 under 35 U.S.C. §103(a). Reconsideration in light of the remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected (1) claims 1-6, 10, 11-16, 20-26, and 30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,381,533 issued to Peleg et al. ("Peleg") in view of U.S. Patent No. 6,397,296 issued to Werner ("Werner"), and (2) claims 7-9, 17-19, and 27-29 under 35 U.S.C. §103(a) as being unpatentable over Peleg in view of Werner and further in view of U.S. Patent No. 6,272,598 issued to Arlitt ("Arlitt").

Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Peleg discloses a dynamic flow instruction cache memory organized around trace segments independent of virtual address line. A computer includes a central processing unit, a cache memory, and a line buffer (Peleg, col. 5, lines 18, 20-21, 44-45, 63-64; Figure 1, elements, 20, 21, 22, and 23). All cache memory inputs are from the line buffer. When the instruction in a basic block are not found in the cache memory, they are obtained from the main memory and executed (Peleg, col. 8, lines 59-65, col. 9, lines 23-27).

Werner discloses a two-level instruction cache for embedded processors. A cache system includes an L1 cache, an L0 cache, and an assist cache. An assist filter is used with the assist

cache (Werner, col. 3, lines 62-65). The artist cache has a victim cache and a prefetch cache. The victim cache includes a first set of cache lines for storing instructions that were displaced from the L0 cache (Werner, col. 4, lines 13-16). The assist filter includes a victim filter and a prefetch filter. The victim filter has a victim memory for storing a set of addresses or tags. The victim cache is responsive to the victim filter (Werner, col. 4, lines 13-22). The victim filter stores the most frequently accessed cache lines in the victim cache (Werner, col. 8, line 67 to col. 9, lines 1).

Arlitt discloses a web cache performance by applying different replacement policies to the web cache. A Least Frequently Used (LFU)-Aging replacement policy replaces the least frequently used object, avoiding cache pollution. The LFU component of the replacement policy maintains a frequency count for each object in the cache. The aging component avoids cache pollution by reducing the frequency count of each cached object by a factor of two whenever the average frequency count exceeds a threshold parameter (Arlitt, col. 6, lines 41-49).

Peleg, Werner, and Arlitt, taken alone or in any combination, does not disclose, suggest, or render obvious (1) transfer of a trace, (2) a first cache to evict the trace based on a replacement mechanism, and (3) a second cache to receive the evicted trace based on a number of accesses to the trace as discussed above. There is no motivation to combine Peleg, Werner and Arlitt because none of them addresses the problem of trace cache filtering. There is no teaching or suggestion that a second cache to receive the evicted trace based on number of accesses is present. Peleg, read as a whole, does not suggest the desirability of filtering trace cache.

Peleg merely discloses obtaining instructions form the main memory if they are not found in the cache. Peleg does not disclose a cache management logistics to control a transfer of a trace. Element 20 is a computer which includes the execution unit and the cache, not a cache management logistics. Werner merely discloses a victim filter storing the most frequently accessed cache lines in the victim cache, not to receive the evicted trace based on number of accesses. The most frequently accessed cache lines are not evicted trace. In fact, Werner essentially teaches away from the invention because while Werner teaches storing, the claims recite evicting. "Storing" and "evicting" are two opposite operations. Arlitt merely discloses use of a threshold to reduce the frequency count by two whenever the average frequency count exceeds the threshold. The threshold is used to reduce the frequency count, not to transfer a

trace. Furthermore, the threshold is used to compare with the average frequency count, not the number of accesses to the trace. In contrast, claims 7, 17, and 27 recite the trace being transferred from the second cache to the L2 cache when a second threshold value is less than a second number of accesses to the trace.

The Examiner states that cache miss reads on this limitation, since a line is needed to evict to free up a space for a new entry (Office Action, page 5, second paragraph). Applicants respectfully disagree. First, a cache miss does not necessarily result in evicting a trace. Peleg merely discloses obtaining the instructions not found in cache from the memory when there is a cache miss. Peleg does not disclose or suggest evicting a trace when obtaining the instructions from the memory. Second, Peleg does not suggest a second cache to receive the evicted trace based on number of accesses to the trace.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §102(b), and 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: November 30, 2004 By

Thinh V. Nguyen
Reg. No. 42,034
Tel.: (714) 557-3800 (Pacific Coast)

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☐ *deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.*

Date: November 30, 2004

FACSIMILE

☒ *transmitted by facsimile to the Patent and Trademark Office.*

November 30, 2004

Tu Nguyen *Date*